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Product Brief

Structera™ A 2504 Memory-Expansion Controller

CXL 2.0 DDR5 4-channel accelerator

P/N MV-SLA25041-A0-HF350AA-C000

Overview

The Marvell® Structera™ A 2504 (P/N MV-SLA25051-A0-HF350AA-C000) device is a CXL near-memory accelerator designed to optimize memory access performance in memory-intensive environments by strategically bringing memory closer to processors and accelerators. This advanced solution enhances memory bandwidth and capacity, better enabling systems to excel at demanding computational tasks.

The Structera A 2504 accelerator supports DDR5 memory up to 6400MT/s, enabling a total of eight DDR5 DIMMs per controller and a maximum memory capacity of 4TB.

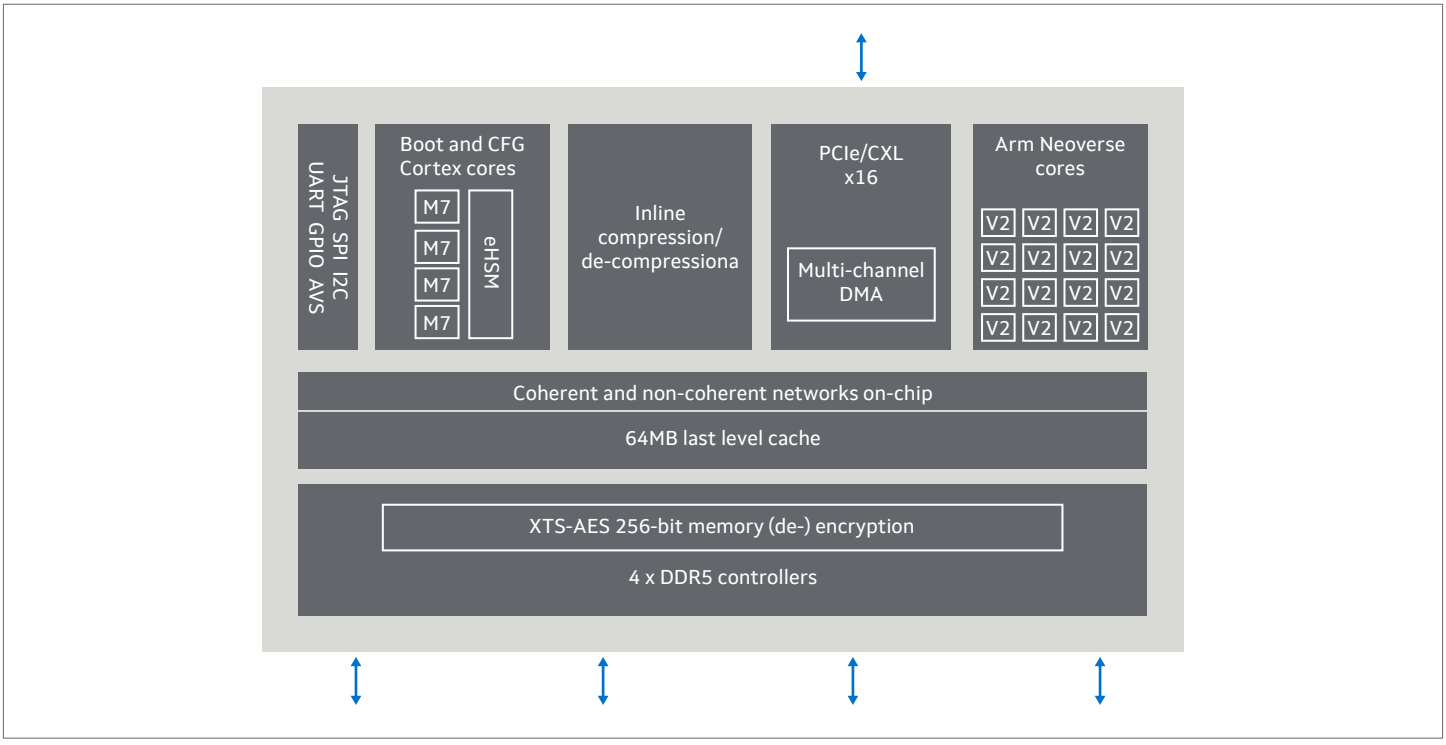
The Structera A 2504 device contains 16 Arm® Neoverse® V2 processor cores and acts as a "server within a server," processing time-sensitive tasks such as AI inference, deep learning recommendation models (DLRM), and in-memory databases on behalf of the primary server processor. By locating processing power next to an additional pod of memory inside of a server, the Structera A 2504 accelerator reduces the time-to-completion, power consumption, and the cost of performing latency-sensitive applications.

The Structera A 2504 device is CXL 2.0 compliant and supports 16 PCIe/CXL lanes for a single host. It offers four inline LZ4 compression engines that support four channels of DDR5-3200 at full bandwidth. The compression engines support both 4KB and 1KB page sizes.

Structera A 2504 accelerator supports inline XTS-AES 256-bit encryption and decryption, ensuring robust data security with high-performance encryption algorithms for sensitive.

The Structera A 2504 device integrates an embedded hardware security module (eHSM) for system-level security. The eHSM securely manages cryptographic keys and provides hardware-based authentication. Coupled with secure boot capabilities, the eHSM ensures that only trusted firmware and software are loaded during system startup, safeguarding against unauthorized access and potential threats.

Block Diagram



Key Features

Features	Details
Standards and interfaces	• PCIe 5.0 (2.5/5.0/8.0/16.0/32.0 GT/s) • CXL 2.0 (8.0/16.0/32.0 GT/sec) • PCIe/CXL host interfaces • 16-lane physical interface (PHY)
CXL modes	• CXL 1.1 Exclusive Restricted CXL Device (eRCD) mode - Power-saving modes - Lane-reversal - Spread-spectrum clocking for common reference-clock links - QoS telemetry
CPU subsystem	• Based on Armv9.0-A and Armv8.5-A • High-performance out-of-order (OOO) architecture with 16 high-performance Arm® Neoverse V2 cores to reduce data movement and enhance parallelism • Highly efficient multilevel cache subsystem • Comprehensive security protection with embedded hardware-security module and secure boot via Arm TrustZone® • Hardware floating-point, SIMD, MMU, and virtualization capabilities • Secure operation with three privilege levels, ensuring isolation and compatibility within the Arm software ecosystem
Memory	• Support for DDR5: - Up to 6400 MT/s data rate - Subdivided into two 40-bit subchannels (32 data bits, eight ECC bits) - Up to four physical ranks per subchannel • U/R/LRDIMM and soldered DRAM • DRAM interfaces with enhanced RAS capabilities. • MPAM support for bandwidth partitioning and monitoring • DRAM crypto with XTS-AES 256 on data with optional address scrambling
Control and management	• Miscellaneous I/O interfaces: SPI/QSPI/xSPI, GPIO, UART, I3C, TWSI, I2C/SMBus • Multiple embedded Arm Cortex M7 processors - System-control processor (SCP) - Management-control processor (MCP) - Cryptographic-control processor (CCP) - PCIe configuration-offload processor (PCP) • Embedded hardware security module (eHSM) using Arm Cortex M3 processor • Extensive power and thermal management capabilities • Compatible with Arm Server Base System Architecture (SBSA)
Compression	• Support for four channels of DDR5-3200 at 100% bandwidth • Support for 4K or 1K page sizes • LZ4 algorithm support • Data integrity protection, including poison and decompress-after-compress
Package characteristics	• 35mm x 35mm package with 0.8 mm ball pitch

Target Applications

- AI/ML inference
- Deep learning recommendation engine model (DLRM)
- High-performance computing (HPC)

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To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies over 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

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